TM-746
2500.000
October 1977

A HIGH RATE AMPLIFIER-DIGITIZER SYSTEM FOR LIQUID ARGON CALORIMETERS

T. F. Droege
Fermi National Accelerator Laboratory *
P. O. Box 500, Batavia Ill.

F. Lobkowicz and Y. Fukushima
University of Rochester
Rochester, New York

Abstract

A low cost charge amplifier for a liquid argon photon detector and a new method for pulse height analysis are described. This scheme is suitable for high energy photon detection with high counting rate. Samples of preamplifier output are taken just before and just after the arrival of the charge from the detector. The difference of these samples provides a stable pedestal and rejects low frequency noise. Short two-pulse resolving time (≈200ns) is achieved.

Introduction

Optimal transformer coupling amplifier schemes for liquid argon detectors have been used for some time. [1,2,3,4]

Transformer coupling is characterized by low noise since the detector is matched to the amplifier. Unfortunately, these transformers are difficult to make and thus expensive. Transformers add an additional complication in that they store energy and thus affect the two pulse resolution.

For high energy photon detection (>10GeV) with high counting rate, short two pulse resolving time is crucial. Since relatively large charge is produced by high energy photons, noise requirements can be less stringent if detector capacitance is kept small. Thus direct coupling schemes can be used to achieve short two pulse resolving time. The amplifier and pulse height analysis system described here is optimized for high counting rate. The two pulse resolving time can, in principle, approach the detector charge collection time.

The basic detector is illustrated in Figure 1. The detector consists of 61 cells which are alternating layers of .080" thick lead and .063" thick copper-clad G-10 boards separated by .080" of liquid argon. The detector has 25 radiation lengths in total. A negative high voltage (3-5kV) is applied to the lead plates and the electron charge is collected on the G-10 boards. An incident photon of 100GeV energy will produce a total collectable charge of 20pc. The G-10 boards are subdivided into ½" wide strips, permitting measurement of the photon position. Each set of strips behind each other is read out by one amplifier; a total of 480 channels are required. Each set of strips has a capacitance of ≈2nf.

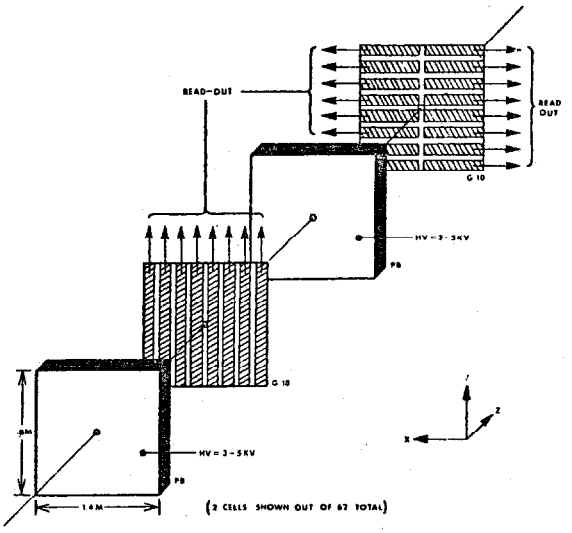


Fig. 1. Configuration of Liquid Argon Shower Detector.

The following conditions influenced the design of the system:

1) A high counting rate - up to 10^5 photons/second - has to be accomodated by the system. Most of these photons will be indicent on the strips near the detector's center. Thus a counting rate of $3\text{-}5\times10^4$/second in each channel is to be handled by the system. Only a small fraction - 10-30/second - of these will actually be digitized. This implies that a pulse should be measurable to a few percent accuracy even if preceded by another pulse in less than 0.3 microseconds.

2) The detector capacitance is 2-2.5nf depending on which strip is read out. This affects both risetime and noise.

3) The energy resolution is better than 11% at 1 GeV incident photon energy.

One would like to detect 1 GeV/channel without significant degrading of the energy resolution by amplifier noise. Thus the rms noise value shold be 10^{-14}C. Because of the relatively large charge produced by high energy photons (>10 GeV), this requirement is less stringent than for most other similar systems.

*Operated by the Universities Research Assoc., Under Contract with the U.S.Dept. of Energy

Pulse Shaping Suitable For High Counting Rates

The intrinsic risetime of the charge pulse arriving at the amplifier is governed by the drift velocity of electrons in argon. Even if one adds methane to the argon to increase the electron mobility, one can only achieve a risetime of ≈100ns for a large detector.

While an input transformer reduces the amplifier noise, the limited low frequency response of practical transformers tends to force the use of bipolar shaping networks. This doubles the potential two pulse resolving time due to rise time.

The approach used here evades this problem by sampling the baseline at t_1 before the arrival of the pulse, as well as at t_2 near the peak of the unclipped pulse, as shown in Figure 2a. If the pulse falls off exponentially like $e^{-\lambda t}$, with $\lambda\tau_0 << 1$, then a single pulse of equal height preceding the measured pulse by a time $t > \Delta t = (t_2 - t_1)$ produces a fractional error.

$$\Delta = e^{-\lambda t} \Delta t$$

while a random pulse rate R of equal height pulses produces an average fractional error

$$(\Delta) = \frac{R\lambda\Delta t}{R+\lambda}$$

for all but the $2R\,\Delta t$ fraction of the pulses which cannot be analyzed at all. We have chosen a time interval $\Delta t = 250$nsec. With a falltime $1/\lambda = 50\mu$sec and a rate $R \approx 5 \times 10^4$/sec the mean error is less than 0.5% except for the 2.4% of unanalyzable events. The double sampling worsens the signal/noise ratio by a factor of $\sqrt{2}$; this is tolerable since the design noise figure is achievable using a low-cost FET at the input.

Because of the possibility of large base line shifts the scheme described here has to be linear over a large pulse-height range. Note that the average baseline shift is $R/2 = 2.5$ times the average pulse height.

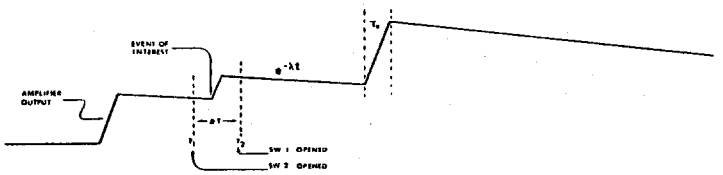
Amplifier Circuit Details

The amplifier circuit card (Figure 2b) consists of a charge sensitive amplifier, a delay line, a fast trigger pick-off amplifier, two track and hold circuits, a difference amplifier, and an output multiplexer. The charge sensitive amplifier is designed to have large dynamic range (10/1) compared to the largest expected input pulse. When this is done, the fall time constant can be made quite large (1000 x rise) with little chance of exceeding the dynamic range since the maximum value of RF is determined by the output range and the average input current.

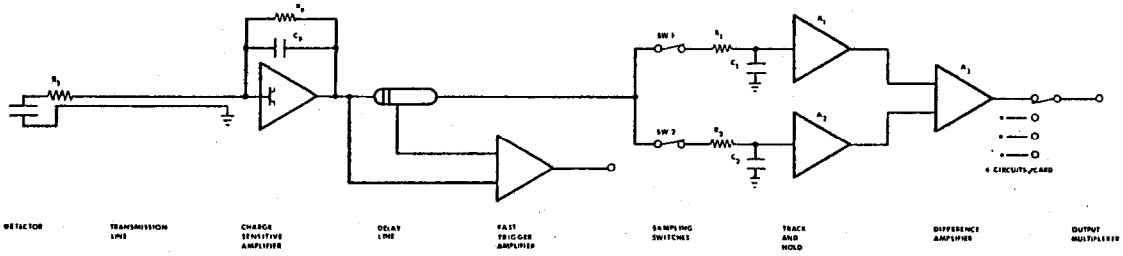
The amplifier output is delayed by a small commercial 400 nanosecond delay line to allow time for trigger decision making from a fast output which is generated by a difference amplifier looking at the input and a tap on the delay line.

If the event is of interest, SW1 is opened just prior to the pulse arrival and C1 stores the base line. After a suitable time, dependent on the RC time constants chosen and the required two pulse resolution, SW2 is opened and the signal is stored as the difference in charge between C1 and C2. While SW1 and SW2 need to be fast, the following amplifiers can be quite slow if they conserve charge.

Recently available CMOS operational amplifiers such as the RCA CA3140, fulfill this requirement quite nicely with practical values allowing storage for several milliseconds with negligible error, adequate for most readout systems.



(a)



(b)

Fig. 2. a) Waveform of preamplifier output showing samples taken at interval Δt around signal with risetime τ_0.
b) Block diagram of electronics.

The circuit is capable of resetting quickly if the event is later determined to be uninteresting since it is only necessary to reclose the switches for the circuit to start tracking a new event.

A1, A2, and A3 are configured as a three amplifier instrumentation amplifier[5] which features excellent common mode rejection so that measurement is not affected by the amplifier output level.

The amplifier circuit (Figure 3) is a conventional charge sensitive amplifier optimized for good rise time with 3nf detector and cable capacitance. An input transformer is not used to match the detector capacitance to the amplifier because it is difficult to make transformers with sufficient rise time that do not ring and thus disturb following signals. Another way to match the detector capacitance to the amplifier capacitance and thus reduce noise by transferring more of the collected charge into the amplifier would be to use many input transistors in parallel. This is not a practical solution in this case since about 100 transistors would be required to match a practical transformer. Still, some improvement is possible by selecting as an input transistor a device designed as a low resistance switch. Such devices are essentially the same construction as transistors commonly used in low noise amplifiers such as the TIS75 but have a repeated geometry. In essence, they are several parallel transistors in the same package. Unfortunately, to achieve the noise redution of many transistors in parallel it is required to operate the transistor at a current level many times that of a conventional transistor. So while there are low cost transistors (for example, the Siliconix E-107) available which can be operated for brief periods to achieve a noise level equivalent to 5-10 TI-S75 transistors in parallel, such use is not practical since operating power levels are exceeded. Perhaps accelerators with short duty cycles could take advantage of the noise reduction possible with these devices by operating with pulsed power supplies. For this amplifier a medium area device, the Siliconix E-110, was chosen and is operated at a 40ma bias current to achieve about 1.5 x improvement in noise compared to devices such as the TI-S75 in our configuration.

The input amplifier was designed to have a 70ns rise time, so it would not contribute significantly to the rise time of the system. To achieve the shortest possible rise time, the inductance of the connecting cable to the detector is kept small. It appears as a transmission line connected to the summing junction of an operational amplifier with the detector capacitance shorting the remote end.

Since this cable is a two meter long 10 ohm low loss printed circuit there is a tendency for oscillation unless a termination is used in the detector.

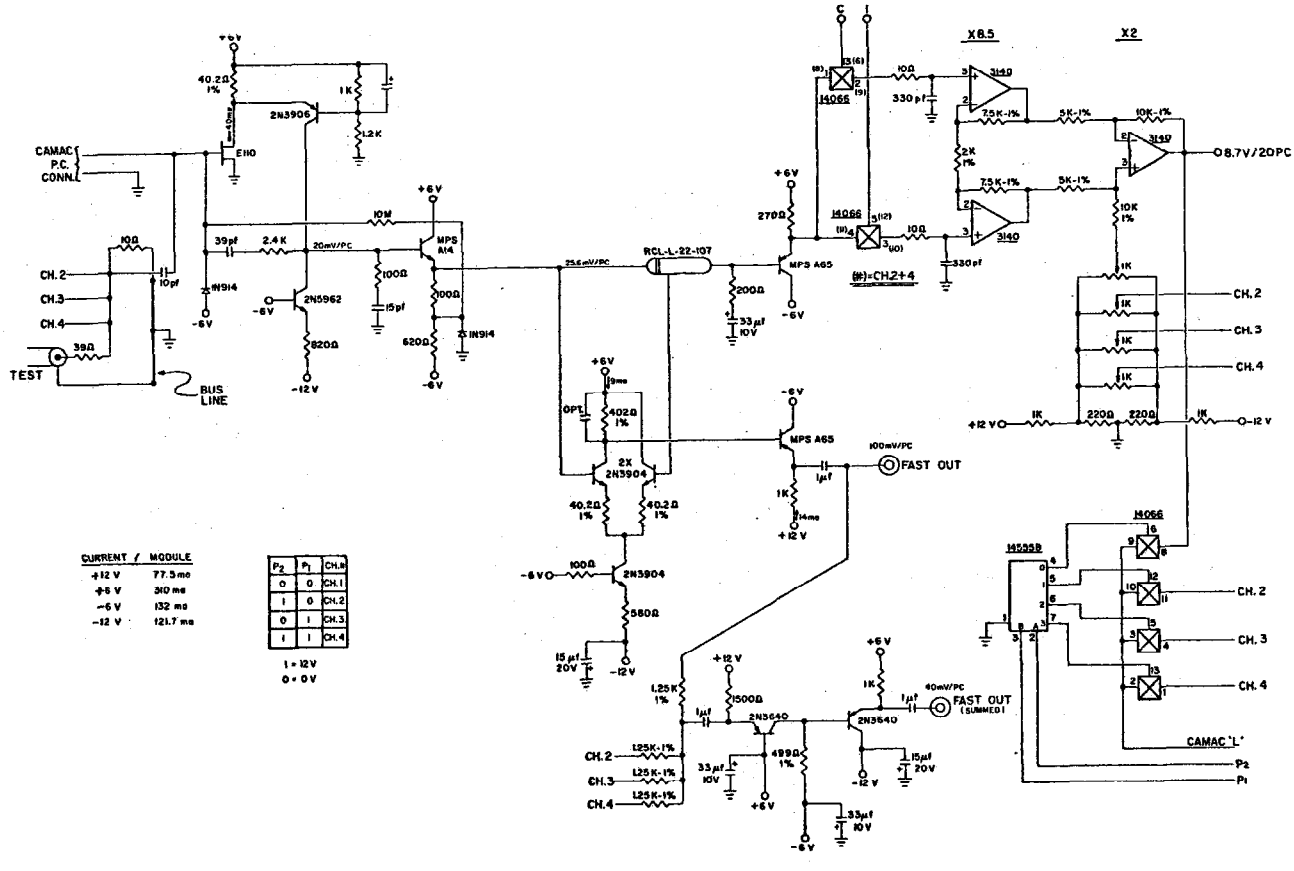


Fig. 3. Detailed Circuit Schematic for Four Channel Amplifier Card.

A tap on the delay line allows a simple difference amplifier to generate a fast linear output for use in the system trigger. These outputs are summed on each four amplifier card for later summation of the total energy. The single channel outputs are further processed by logic circuits for selection of the number of bunches in the final trigger.

Read Out System

In order to reduce engineering time the amplifier and read out system is packaged on CAMAC [6] cards and uses standard CAMAC crates with non-standard power supplies. The bus use is completely non-standard, however. Twenty-three four channel amplifier cards and a scanner can be mounted in each crate - (Figure 4). The scanners from several crates (presently 6) are interconnected by a bus which contains only control signals. A NIM module which contains the single system Analog to Digital Converter (ADC) controls the data scan and accepts an analog signal cable from each scanner.

A system trigger starts the read-out scan. The controller triggers the scanners which through CAMAC bus lines select channel Ø on all amplifier modules. The amplifier modules connect their channel Ø analog output to their CAMAC "L" line. After sufficient settling time the scanner module steps through the "L" lines comparing the signal to an analog threshold which is distributed to the scanners. When an over threshold signal is found, the analog level is connected to the ADC module and a settling time wait is initiated.

After initiating the sequence, the ADC module continously scans the scanner modules in sequence looking for one with a signal for conversion. When one is found it is only necessary to wait for the settling time of one switching operation inside the ADC module before starting the analog to digital conversion.

Since a number of analog scanning operations proceed in parallel, the total scanning and conversion time is little more than the scanning time for a single crate.

The ADC module stores the result of each conversion along with the channel, card, crate address, and a scan completed bit in a FIFO CAMAC buffer memory for access by the experiments data collection computer.

Performance

The amplifier circuit has a typical rms noise figure of 7×10^{-15}C without selection of the input FET when used with a 3nf detector and with 34db two pulse rejection at 200ns. Some trade off between noise and two pulse resolution is possible by adjusting the time constants in the track and hold circuits.

The circuit is linear from zero up to an input of 17 pc, corresponding to a photon energy/channel of 85 GeV. Because of the subdivision of the detector each photon distributes its energy over 5-8 channels; thus the circuit is linear as long as the total energy deposited does not exceed 425 GeV. Since the highest expected photon energy will be $\leq$250 GeV, and the typical photon energy is $\approx$50 GeV, the circuit is within its limits even at the highes expected counting rate.

Figure 5 shows the two pulse resolution of the system measured directly by sampling one of two equal fast pulses separated by the time internal Δt. Figure 6 shows in detail the expected error produced by a single equal height pulse preceding the measured pulse by a given time interval.

This scheme is a compromise designed to instrument a large number of channels at relatively low cost. It suffers by a $\sqrt{2}$ noise factor due to the two sample measurement and an even larger factor because it is difficult to build a satisfactory transformer for matching the amplifier to the detector capacitance.

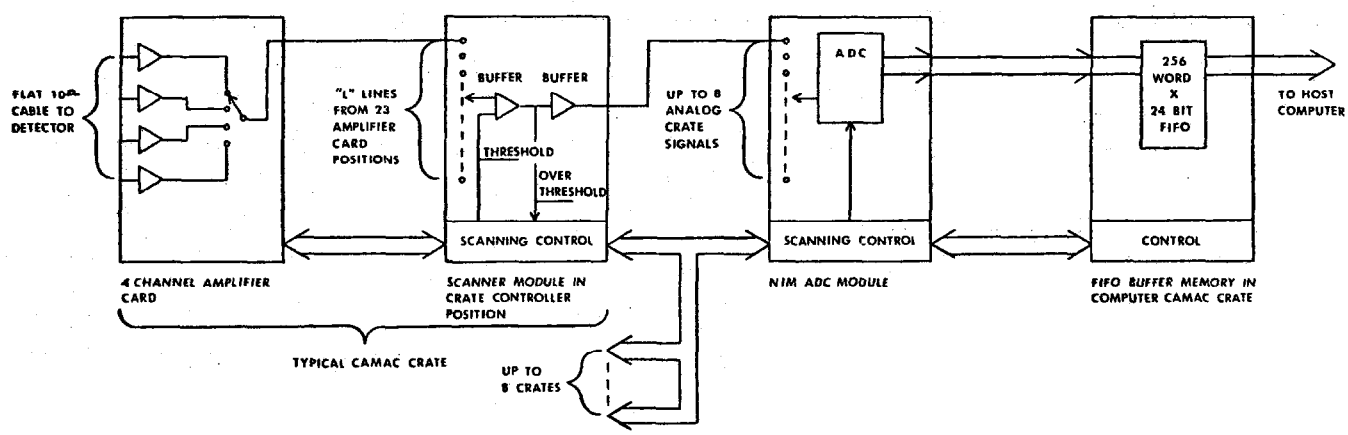


Fig. 4. Block Diagram of Amplifier Crates with Read Out System

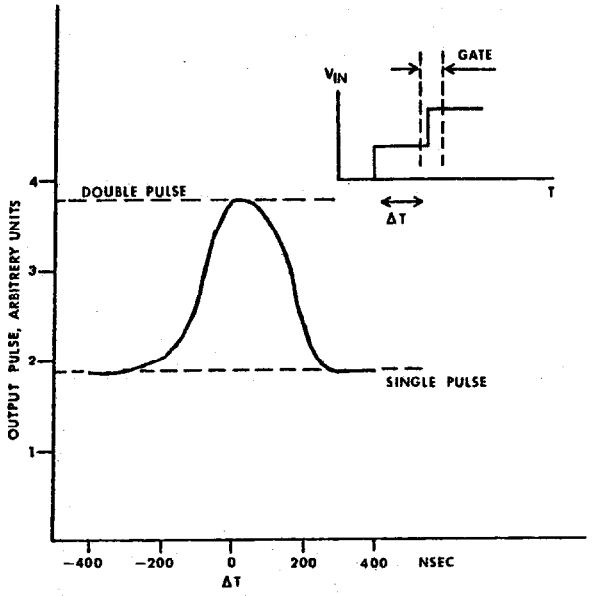


Fig. 5. System Two Pulse Resolution.

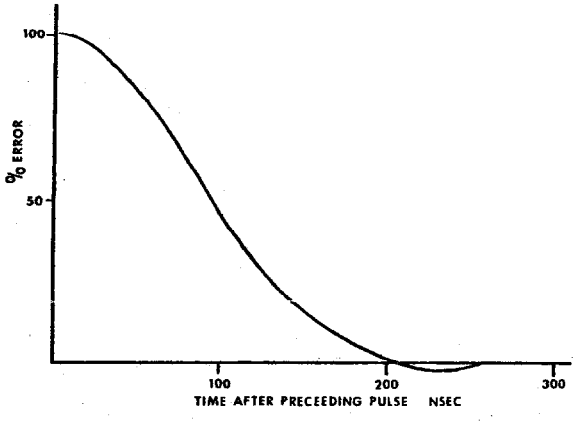


Fig. 6. Error Produced by a Single Equal Height Pulse Preceding the Measured Pulse.

If the lowest possible noise figure is not needed, then this scheme has some advantages over the more conventional designs which differentiate to produce a pulse which is then transmitted to a peak-sensing ADC or sample-hold circuit. First, there is a cost saving due to elimination of the differentiating circuitry. By designing the sample and hold circuits to be on the same card with the preamplifier the need for long distance transmission of many relatively low level-high speed signals is eliminated. Instead, transmission is performed at slow speed and high level with the long distance transmission after digital conversion.

The two sample technique operating on an integrated charge signal is inherently much easier to implement than linear gate-stretcher or peak detector circuits. Only the switches need be high speed since everything else can be allowed relatively long periods to settle as long as charge is conserved.

Present CMOS switches are fast and economical and while some charge is transferred in the switching operation, this tends to be matched within the same chip, and is relatively stable with temperature. Pedestal stability for this design is excellent since each measurement contains a built-in baseline calibration done in operational amplifier circuits requiring drift stability that is very easy to achieve. The high stability of the pedestal makes it possible to select channels for conversion by comparison to a single threshold for all channels, greatly simplifing the read-out system.

Abort time for this circuit is quite fast since it is only necessary to close the track and hold switches and allow a few switch R, Storage C time constants (Figure 2b) In the present design 150ns are sufficient for tracking to recover to 1%.

The delay line used in each channel is the single most expensive item ($6.55) in this design. By placing this delay on the amplifier card the need for many cable delays, some other storage scheme, or an equivalent dead time restriction, is removed. By placing the delay line on the card a high impedance line can be used which minimizes cross-talk problems. A tap on the delay line is a convenient means to generate a test signal for use in the trigger.

Parts and assembly cost for the amplifier cards, not including check-out and test, is $40.00 per channel.

References

1. W.J. Willis and V. Radeka, Nucl. Instr. & Meth. 120, (1974) 221

2. J. Engler et. al., Nucl. Instr. & Meth. 120, (1974) 157

3. D. Hitlin et. al., Nucl. Instr. & Meth. 137, (1976) 225

4. C.W. Fabjan et. al., Nucl. Instr. & Meth., 141, (1977) 61

5. G.E. Tobey et.al., Operational Amplifiers, McGraw Hill, New York, N.Y., 207

6. "CAMAC, A Modular Instrumentation System for Data Handling", USAEC, TID-25875, July, 1972